

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: **Taylor R. Efland**

Docket No.: **TI-30963.1**

Serial No.: **TBD**

Examiner: **TBD**

Filed: **Herewith**

Art Unit.: **TBD**

For: **Thermally Enhanced Semiconductor Chip Having  
Integrated Bonds Over Active Circuits**

Conf. No.: **TBD**

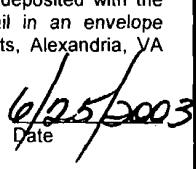
**INFORMATION DISCLOSURE STATEMENT**

Assistant Commissioner For Patents  
Alexandria, VA 22313-1450

**MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(A)**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Alexandria, VA 22313-1450.

  
Elizabeth Austin

  
Date

Dear Sir:

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed PTO-1449. Copies of the listed references are enclosed.

This information disclosure statement is being mailed before receipt of a first office action on the merits in accordance with 37 C.F.R. 1.56, 1.97, and 1.98.

No fees are due. However, should the Office decide otherwise, please charge the necessary fee to the deposit account of Texas Instruments Incorporated, Account Number 20-0668.

Respectfully submitted,



Michael K. Skrehot

Attorney for Applicants

Reg. No. 36,682

Texas Instruments Incorporated  
P. O. Box 655474, MS 3999  
Dallas, Texas 75265  
(972) 917-5653

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Substitute for Form 1449A/PTO  
**INFORMATION DISCLOSURE  
 STATEMENT BY APPLICANT**  
 (use as many sheets as necessary)

				Complete If Known
				Application Number. <i>TBD</i>
				Filing Date. <i>Herewith</i>
				First Named Inventor. <i>Taylor R. Efland</i>
				Group Art Unit. <i>TBD</i>
				Examiner Name. <i>TBD</i>
Sheet	1	of	2	Attorney Docket No. <i>TI-30963.1</i>

**U.S. PATENT DOCUMENTS**

Exam. Initials *	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
AA	4,259,685			Romano	03/31/1981	
AB	4,518,982			DuBois, et al.	05/21/1985	
AC	5,610,442			Schneider, et al.	03/11/1997	
AD	5,753,974			Masukawa	05/19/1998	
AE	6,075,289			Distefano	06/13/2000	
AF	4,346,396			Carroll, II, et al.	08/24/1982	
AG						
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AJ						
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**FOREIGN PATENT DOCUMENTS**

Exam. Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>2</sup> (if known)				
	BA							
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<sup>1</sup>Unique citation designation number. <sup>2</sup>See attached Kinds of U.S. Patent Documents. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

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**INFORMATION DISCLOSURE  
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Sheet

2

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		Complete If Known	
		Application Number	TBD
		Filing Date	Herewith
		First Named Inventor	Taylor R. Efland
		Group Art Unit	TBD
		Examiner Name	TBD

Attorney Docket No. TI-30963.1

**OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS**

Exam. Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	CA	"Controlled Collapse Reflow Chip Joining", L. F. Miller, IBM J. Res. Develop., Vol. 13, May 1969, pp. 239-250	
	CB	"Geometric Optimization of Controlled Collapse Interconnections", L.S. Goldman, IBM J. Res. Develop., Vol. 13, May 1969, pp. 251-265	
	CC	"Paramedic Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques", Sevgin Oktay, IBM J. Res. Develop., Vol. 13, May 1969, pp. 272-285	
	CD	"Reliability of Controlled Collapse Interconnections", K.C. Norris and A.H. Landzberg, IBM J. Res. Develop., Vol. 13, May 1969, pp. 266-271	
	CE	"SLT Device Metallurgy and Its Monolithic Extension", P.A. Totta and R.P. Sopher, IBM J. Res. Develop., Vol. 13, May 1969, pp. 226-238	
	CF	"Studies of the SLT Chip Terminal Metallurgy", B.S. Berry, and I. Ames, IBM J. Res. Develop., Vol. 13, May 1969, pp. 286-296	
	CG		
	CH		
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